



Liu, D., Hollis, S., & Stark, B. (2019). A new design technique for sub-nanosecond delay and 200 V/ns power supply slew-tolerant floating voltage level shifters for GaN SMPS. *IEEE Transactions on Circuits and Systems - I: Regular Papers*, 66(3), 1280-1290. [8535039].  
<https://doi.org/10.1109/TCSI.2018.2878668>

Publisher's PDF, also known as Version of record

License (if available):  
CC BY

Link to published version (if available):  
[10.1109/TCSI.2018.2878668](https://doi.org/10.1109/TCSI.2018.2878668)

[Link to publication record in Explore Bristol Research](#)  
PDF-document

This is the final published version of the article (version of record). It first appeared online via IEEE at <https://ieeexplore.ieee.org/document/8535039> . Please refer to any applicable terms of use of the publisher.

## University of Bristol - Explore Bristol Research

### General rights

This document is made available in accordance with publisher policies. Please cite only the published version using the reference above. Full terms of use are available:  
<http://www.bristol.ac.uk/red/research-policy/pure/user-guides/ebr-terms/>

# A New Design Technique for Sub-Nanosecond Delay and 200 V/ns Power Supply Slew-Tolerant Floating Voltage Level Shifters for GaN SMPS

Dawei Liu<sup>ID</sup>, Simon J. Hollis, *Member, IEEE*, and Bernard H. Stark<sup>ID</sup>

**Abstract**—Dual-output gate drivers for switched-mode power supplies require low-side reference signals to be shifted to the switch-node potential. With the move to ultra-fast switching GaN converters, there is a commercial need to achieve switch-node slew-rates exceeding 100 V/ns, however, reported level shifters do not simultaneously achieve the required power supply slew immunities and sub-ns propagation delays. This paper presents a novel design technique to achieve the first floating voltage level shifters that deliver slew-rate immunities above 100 V/ns and sub-ns delay in the same circuit. Step-by-step transistor-level design methods are presented. This technique is applied to improve a reported level shifter, and experimentally validated by fabricating this level shifter in a 180 nm high-voltage CMOS process. The final level shifter has zero static power consumption, and is shown to have a sub-nanosecond delay across the whole operating range, a 200 V/ns positive power-rail slew tolerance, and infinite negative slew tolerance. The measured propagation delay decreases from 722 ps with the floating ground at  $-1.5$  V, to 532 ps for a floating ground of 45 V, and the power consumption is 30.3 pJ per transition at 45 V. It has a figure of merit of 0.06 ns/( $\mu$ mV), which is an 1.7 $\times$  improvement on the next best reported level shifter for this type of application.

**Index Terms**—Area efficient, energy efficiency, floating voltage level shifter, GaN, gate driver, high speed, low power, slew tolerance.

## I. INTRODUCTION

THE figure of merit (FOM) of Gallium Nitride (GaN) power FETs is superior to that of silicon FETs [1]. Multi-MHz switching [2]–[5] GaN FETs are therefore widely seen as the next generation of power electronic devices for sub-1kV applications, as they offer increased speed, efficiency and power density [6]. Their introduction enables smaller and more efficient switched-mode power supplies (SMPS). However, this development depends on gate drivers being able to drive GaN FETs at speeds of 100 V/ns and beyond, which

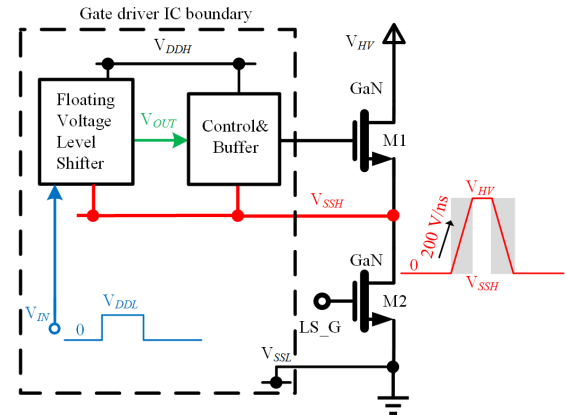


Fig. 1. The level shifter developed here lies between the input of the gate driver and the high-side driver stage for a dual-output gate driver. Its input  $V_{IN}$  is ground-referenced, and its output  $V_{OUT}$  is referenced to the  $V_{SSH}$  rail that slews at up to 200 V/ns in a GaN FET bridge leg converter.

is 1 to 2 orders of magnitude faster than switching speeds used for similarly rated silicon power FETs or IGBTs.

This fast driving is especially challenging on the high-side of a bridge leg, as illustrated in Fig. 1. The control input signal  $V_{IN}$  to the dual-output driver shown is referenced to ground  $V_{SSL}$ . The floating-voltage level shifter provides a level-shifted copy of  $V_{IN}$  (labelled  $V_{OUT}$ ) to the high-side control and buffer circuits, which are referenced to the switch-node voltage  $V_{SSH}$ . The desired increase in switching speed of GaN devices therefore comes with a requirement to ensure that level shifter's slew immunity equals or exceeds the desired slew rate of the switch-node, or else the level-shifted signal  $V_{OUT}$  may contain errors. Examples of reported level-shifter slew-rates of are 50V/ns in [2] and [4], 75V/ns in [5], and 120 V/ns in [7].

The move to higher switching speeds also leads to higher switching frequencies, which therefore requires level shifters with reduced propagation delay, ideally sub-ns [2], [3], and reduced low power dissipation per transition. The combination of low delay and high slew immunity is difficult to achieve, for example the 120 V/ns capable level shifter of [7] has a 20 ns propagation delay. For these reasons, new level shifter designs are needed with higher slew immunity and lower propagation delay, to enable commercial gate drivers to that can fully exploit the high switching speed of GaN FETs.

Manuscript received June 24, 2018; revised September 27, 2018 and October 16, 2018; accepted October 17, 2018. This work was supported by the U.K. Engineering and Physical Sciences Research Council (EPSRC) under Grants EP/K021273/1 and EP/R029504/1. This paper was recommended by Associate Editor A. Fayed. (Corresponding author: Dawei Liu.)

D. Liu and B. H. Stark are with the Faculty of Engineering, University of Bristol, Bristol BS8 1UB, U.K. (e-mail: dawei.liu@bristol.ac.uk; bernard.stark@bristol.ac.uk).

S. J. Hollis is with Xilinx, San Jose, CA 95124 USA (e-mail: harryhollis@cantab.net).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TCSI.2018.2878668

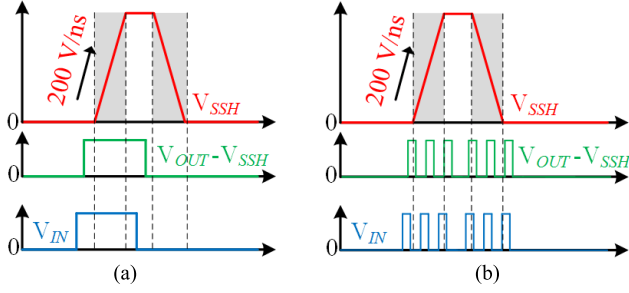


Fig. 2. Two level shifter application scenarios: (a) Input signal  $V_{IN}$  transition lies outside of  $V_{SSH}$  slewing period, (b) input signal transitions lie within the slewing period.

This paper presents a validated design method for floating level shifters with up to 200 V/ns slew immunity and sub-ns propagation delay. The method is applicable to level shifters in applications where the input signal transitions lie *outside* of the slewing periods [2]–[5], as illustrated in Fig. 2 (a). In this scenario, the presented design method achieves a 200 V/ns positive slew-rate immunity and an infinite negative slew-rate immunity. This is a 70% improvement in the figure of merit over reported high-voltage floating level shifters to  $0.53 \text{ ns}/(0.18 \mu\text{m} \times 50 \text{ V}) = 0.06 \text{ ns}/(\mu\text{mV})$ . The average propagation delay is 532 ps, and the power consumption is 30.3 pJ per transition for a peak  $V_{SSH}$  of 45 V.

The method can also be applied to applications where the input transitions occur *during* slewing, as illustrated in Fig. 2 (b). An example of this scenario is a dual-output driver whose low-side clock needs to be level-shifted to the high floating side. This is the case, for example, in digital active gate driving, where the driving impedance is modulated digitally during the slewing period to reduce current overshoot [8] or suppress crosstalk [9]. In this second scenario, the proposed method results in a level shifter that achieves 200 V/ns and -60 V/ns slew-rate immunity. Both scenarios have the same average propagation delay (532 ps), and power consumption per transition (30.3 pJ for  $V_{SSH} = 45 \text{ V}$ ).

The paper is organised as follows: Section II reviews reported high-voltage floating level shifters. Section III analyses the pulse-triggering level shifter of [10], to establish a base line. Section IV presents a step-by-step methodology to increase slew immunity whilst maintaining sub-ns delay. Section V compares measured performance against previous work, and Section VI draws conclusions.

## II. STATE OF THE ART HIGH-VOLTAGE FLOATING LEVEL SHIFTERS

The conventional low voltage (LV) to high voltage (HV) level shifter in [11] uses cascaded HV NMOS to protect and clamp the LV input transistors, and HV PMOS to protect and clamp the output floating LV transistors. This class of floating voltage level shifter has a large propagation delay and occupies a large layout area, due to the use of HV NMOS and PMOS as protection devices. The level shifter presented in [12] makes significant improvements in these two aspects. The LV input transistors are removed and the

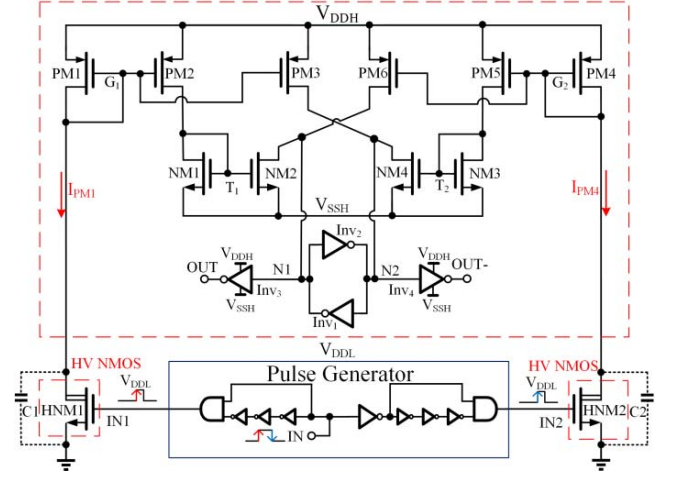


Fig. 3. The base-line pulse-triggered high-voltage floating level shifter of [10] ( $V_{DDL} = (V_{DDH} - V_{SSH}) = 1.8 \text{ V}$ ). Red dashed boxes are deep N-wells).

cascaded HV NMOS transistors are used as the input stage, and a series of optimizations have been given to realise a nanosecond delay time in a  $0.35 \mu\text{m}$  HV-CMOS process. Based on the level shifter in [12], the level shifter in [13] achieves significantly reduced power dissipation and propagation delay through changing the cascaded HV PMOS to HV NMOS, and changing the input to one-shot triggered. However, this level shifter cannot be applied to SMPS drivers, as the floating low-voltage  $V_{SSH}$  needs to remain constant, and cannot go below zero. Another type of high-speed voltage level shifter uses diode-connected and cross-coupled LV PMOS transistors as the load [14], [15]. The drawback is the continuous static power dissipation. In [16] and [17], a device and circuit co-design technique is introduced, where drain-extended MOS (DeMOS) transistors are used, and where the process is optimised to shorten the level shifters' propagation delay. In this way, delays of 0.45 ns and 0.38 ns are achieved, for a 1.2 V to 5 V level shifter. However, this method requires a DeMOS doping profile, which is not normally available in a standard HV CMOS process. A pulse triggered level shifter is presented in [18], but no slew-rate immunity feature is reported.

To improve power rail slew-rate immunity over that of the aforementioned level shifters, a number of techniques have been reported. An overlapping clamping structure is used in [19] to obtain a slew-rate immunity 20 V/ns. The pulse-triggered level shifter of [10] shown in Fig. 3, uses pull-up and pull-down current mirrors to cancel the injected common mode current, whilst not disturbing the input signal.

This level shifter achieves a slew-rate immunity of 30V/ns, with a 370ps propagation delay. In [20], part of the parasitic current induced by power supply slewing is canceled out by two high-side dynamic currents to obtain a slew rate immunity of 40V/ns. In [21], two feedback loops from the level shifter output to input are used to cancel the slew-related influence on the input trigger signals to reach 50V/ns. Finally, Yang *et al.* [7] present a slew rate enhancement technique to achieve 120 V/ns slew rate immunity and a propagation delay of 20 ns.

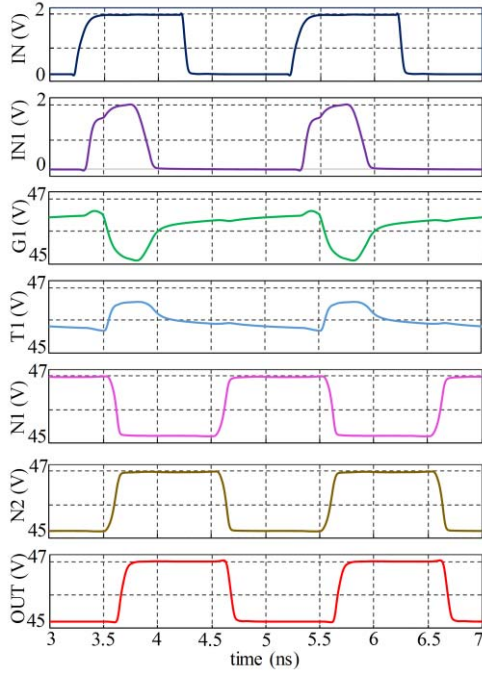


Fig. 4. Transient simulation results of basic level shifter in [10] ( $V_{SSH} = 45$  V,  $V_{DDL} = (V_{DDH} - V_{SSH}) = 1.8$  V).

### III. BASE-LINE CIRCUIT: PULSE-TRIGGERED CURRENT MIRROR-BASED FLOATING VOLTAGE LEVEL SHIFTER

The pulse-triggered current-mirror-based floating level shifter of [10], whose circuit schematic is shown in Fig. 3, forms the starting point for this paper's proposed designs. The transistors in the large dashed box are 1.8V transistors that are isolated from the remainder of the circuit. HNM1 and HNM2 are isolated 50V HV NMOS transistors. On a rising edge of IN, a single high pulse is created at IN1, see the schematic simulation results in Fig. 4. This, in turn, switches on HNM1, pulling G1 low. PM2 switches on, pulling T1 high. This turns NM2 on, pulling N1 low. At the same time, PM3 mirrors the current pulse flowing through PM1, pulling N2 high. In this way, the rising input edge has produced a level-shifted output OUT. On the subsequent falling edge at IN, the same process occurs, however this time on the right-hand-side of the circuit: N2 is pulled down by NM4, and N1 is pulled up by PM6. The states at N1 and N2 are locked by the latch composed of  $Inv_1$  and  $Inv_2$ , ensuring that output OUT will be held the same logic level (referenced to  $V_{SSH}$ ) until the next change at input IN.

As analysed in [10], the design combines the benefits of an energy saving pulse-triggered input, a high-bandwidth current mirror and a full latch to stabilize the output state. This level shifter has a propagation delay of 435 ps when  $V_{SSH}$  is 45V.

The current mirror architecture is also used to enhance slew-rate immunity. Voltage slew at  $V_{SSH}$  generates parasitic currents  $I_{PM1}$  and  $I_{PM4}$  (see Fig. 3), that charge the parasitic capacitances  $C_1$  and  $C_2$ .  $I_{PM1}$  and  $I_{PM4}$  are mirrored to PM3 & NM2 and PM6 & NM4, where the mirrored pull-up and pull-down parasitic currents cancel each other at

nodes N1 and N2 instead of triggering the latch circuit. This design method strengthens the shifter's supply voltage slew immunity. As a result, the base-line level shifter of Fig. 3 can handle a  $V_{SSH}$  slew rate 15 V/ns, confirmed by post-layout simulation.

## IV. DESIGN IMPROVEMENTS AND THE PROPOSED FLOATING VOLTAGE LEVEL SHIFTER

### A. Limitations of the Base-Line Level Shifter in GaN SMPS

The level shifter described in the previous section has two important shortcomings which limit its application in power converters that use GaN FETs. First, the level shifter's floating power supply slew tolerance must be increased to well beyond 100 V/ns. Second, its operating range must be expanded to support  $V_{SSH}$  as low as  $-1.5$  V [22]. This negative  $V_{SSH}$  occurs in the deadtime (the lock-out safety period prior to transitions) when both GaN FET gates are pulled low and the low-side GaN FET (M2 in Fig. 1) is reverse conducting. GaN FETs do not have a body diode [22] and under reverse conduction, the source-drain voltage drop is roughly equal to the device's gate threshold voltage.

### B. Design Overview and Summary Results

Negative  $V_{SSH}$  and slew tolerance will be addressed in four design steps. The first three steps optimize the level shifter for input transients that occur outside of the  $V_{SSH}$  slewing period, and the forth step enables the operation during the slewing period.

- Step 1: Create a new level shifter ("Type I"), capable of operation with  $V_{SSH} \geq -1.5$  V.
- Step 2: Insert cross-coupled current-mirror pairs to increase positive power supply slew tolerance from 14 V/ns to 60 V/ns ("Type II").
- Step 3: Add an auxiliary positive power supply slew immunity enhancement circuit, to improve slew tolerance from 60 V/ns to 200 V/ns ("Type III").
- Step 4: Add an auxiliary negative power supply slew immunity enhancement circuit to reach 200 V/ns and -60 V/ns slew tolerance for operation during the slewing period.

The effects of the refinements on the key post-layout simulated characteristics including rising ( $T_R$ ) and falling ( $T_F$ ) propagation delays, the energy consumption per transition ( $E_T$ ) and power supply slew immunity  $dv/dt$  of the circuits are summarised in TABLE 1.

### C. STEP 1: Type I Level Shifter for Negative $V_{SSH}$ Tolerance

Design Step 1 aims to enable use of negative  $V_{SSH}$ . The drain to source voltage ( $V_{DS}$ ) of HNM1 and HNM2 in Fig. 3 should fulfil  $V_{DS,HNM1} > V_{DDL} - V_{th,HNM1}$  to keep them operating in the saturation region, and ensure sufficient trigger current  $I_{PM1}$ ,  $I_{PM4}$  when the gate voltage pulse arrives.

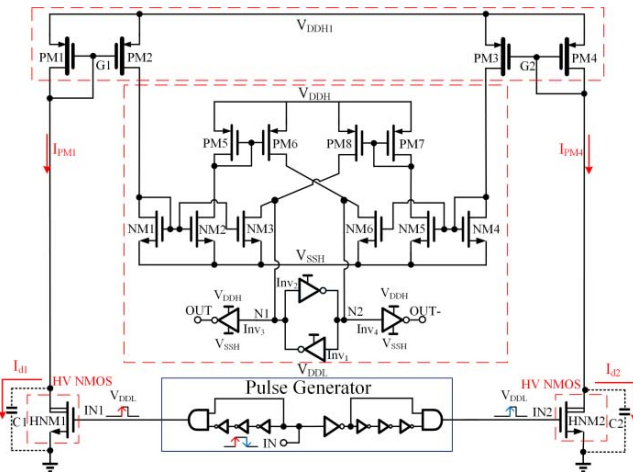
$$I_{PM1} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{DDL} - V_{th})^2 \quad (1)$$



TABLE I

SUMMARY OF LEVEL SHIFTERS' PERFORMANCE WITH  $V_{DDH} = 50V$ , DATA OBTAINED FROM POST-LAYOUT SIMULATION

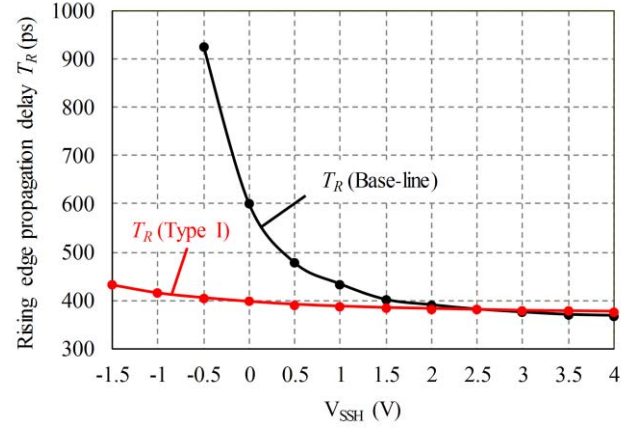
Parameter	$T_R$ (ps)	$T_F$ (ps)	$E_T$ (pJ)	$+dv/dt$ (V/ns)	$-dv/dt$ (V/ns)	$-dv/dt$ (V/ns)
Operating scenario	Outside of $V_{SSH}$ slewing period, see Fig. 2 (a)					During slewing
Base-line	399	435	27.6	15	$\infty$	16
Type I	413	479	30.3	14	$\infty$	20
Type II	505	567	31.8	60	$\infty$	18
Type III	522	584	31.8	200	$\infty$	16
Type IV	541	602	31.8	200	$\infty$	60

Fig. 5. Type I level shifter: the floating high-voltage floating level up shifter with additional  $V_{DDH1}$  power rail ( $V_{DDH1} - V_{SSH} = 5V$ ,  $V_{DDL} = (V_{DDH} - V_{SSH}) = 1.8V$ , red dashed boxes are deep N-wells).

Since  $V_{DS,HNM1} = V_{DDH} - V_{gs,PM1}$ , and  $V_{gs,PM1}$  are larger than  $V_{th,PM1}$ , the minimum value of  $V_{DDH}$  should equal  $V_{DDL}$ , to guarantee that HNM1 operates in saturation and obeys trigger current equation (1). If  $V_{SSH} < 0$  and  $V_{DDH} < V_{DDL}$ , the pulse-trigger current through HNM1 and HNM2 reduces and the level shifter becomes slower. If  $V_{DDH}$  is smaller than  $V_{th,PM1}$ , then the triggered current is close to zero, and the level shifter does not operate correctly.

To solve this problem, another power supply  $V_{DDH1}$  is added, as shown in Fig. 5, resulting in level shifter Type I. This rail feeds two current mirrors made up of transistors PM1 to PM4, which are rated at 5 V, and placed in a new isolation well.  $V_{DDH1}$  is 5 V above  $V_{SSH}$ , so if  $V_{SSH}$  is  $-1.5V$ ,  $V_{DDH1}$  is still 3.5V, which still provides enough triggered current for HNM1 or HNM2 to provide correct operation.

Fig. 6 shows the post-layout-simulated rising propagation delay  $T_R$  against  $V_{SSH}$  of the base-line level shifter (Fig. 3) and the Type I level shifter of Fig. 5. It can be seen that as  $V_{SSH}$  reaches  $-0.5$  V, the propagation delay of the base-line circuit exceeds 900 ps. Below  $-0.5$  V, the base-line level shifter does not operate normally. By contrast, the propagation delay in the Type 1 level shifter remains below 450 ps, even when  $V_{SSH}$  is  $-1.5$  V. The  $T_R$  of the Type I level shifter

Fig. 6. Post-layout simulated rising propagation delay  $T_R$  against  $V_{SSH}$  for the base-line and Type I level shifters.

is slower than that of the base-line level shifter when  $V_{SSH}$  is larger than 3 V. This is because the triggering currents are almost the same for these two level shifters, and the Type I level shifter adds the additional power supply and current triggering path. Further, adding the  $V_{DDH1}$  power rail and 5V PMOS transistors increases Type I level shifter's power dissipation over the Base-line level shifter. In short, the Type I level shifter permits negative  $V_{SSH}$  and improves the propagation delay for  $V_{SSH} < 3V$ .

The Type I level shifter has a similar slew-rate immunity (14 V/ns in post layout simulation) to the base-line level shifter (15 V/ns), since the common mode parasitic currents  $I_{d1}$  and  $I_{d2}$  are still mirrored to nodes N1 and N2 through several current mirrors during a positive slew of  $V_{SSH}$ .

The intended application of this level shifter is to drive a fast, floating gate driver [9] with 1.8 V input logic, and therefore this negative  $V_{SSH}$  is problematic. The Type I level shifter addresses this problem. For gate drivers with 5 V logic, this solution is not needed, as the base-line level shifter could be designed with 5 V transistors and a 5V power supply.

#### D. STEP 2: Type II Level Shifter With Increased $V_{SSH} dv/dt$ Immunity

Design Step 2 aims to improve slew immunity by applying cross-coupling methods reported in [23] and [24]. The slew-rate of the Type I level shifter is limited by slew-induced common-mode current  $I_{cm}$ , which flows through PM1 and PM4 and is mirrored to NM1 and NM4, see Fig. 7(a). In [10], the slew immunity of the latch-triggering current mirror networks composed by PM5-PM8, NM2-NM3 and NM5-NM6 are analysed. leading to the conclusion that the maximum slew rate is limited by excessive  $I_{cm}$  flowing through NM1 and NM4.

In order to inhibit this slew-induced triggering, a Type II level shifter is designed with additional cross-coupled transistors, as illustrated in Fig. 7(b). Crossed-coupled transistors PM9 and PM10 allow half of the common-mode current to bypass PM1 and PM4, thus halving the common-mode current directed towards NM1, NM4, NM7 and NM8. Equally,



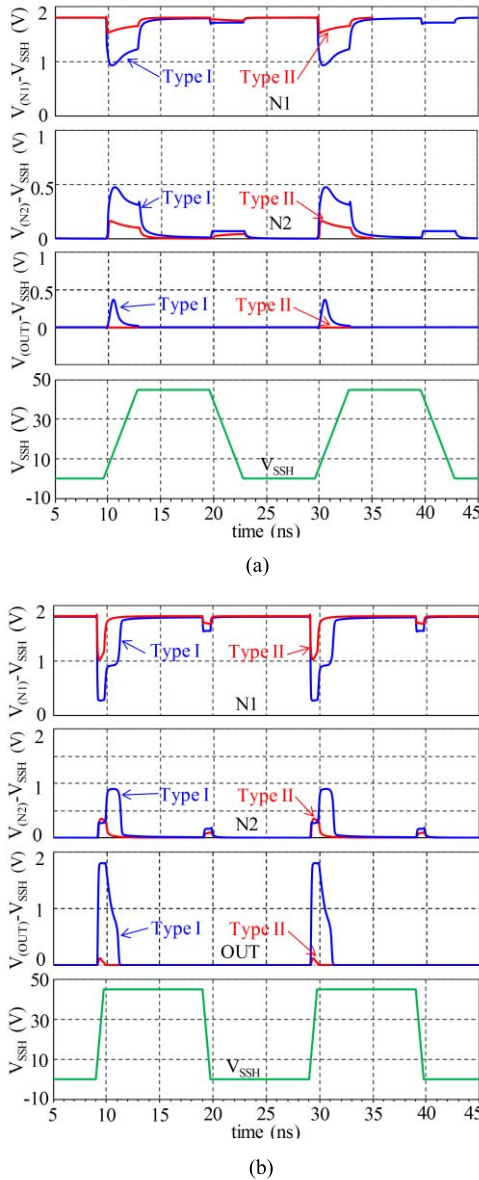


Fig. 9. Transient simulation (post-layout) results for two different  $V_{SSH}$  slew rates, showing node voltages at N1, N2, and OUT, for the Type II and Type I level shifters. Type II demonstrates an improved slew-rate immunity. (a)  $V_{SSH}$  slew rate = 14 V/ns. (b)  $V_{SSH}$  slew rate = 60 V/ns.

mirror circuit,  $I_{NM10}$  equals half of  $I_{d3}$ , and  $I_{PM2}$  equals half of  $I_{PM1}$ , and  $I_{NM1}$  is zero.

As a result, due to the addition of this auxiliary circuit, the slew-induced common-mode current that could trigger the latch is significantly reduced, which means an increased power slew immunity can be achieved.

Transient simulation results of the Type II and Type III level shifters, for a  $V_{SSH}$  slew rate of 200 V/ns, are shown in Fig. 11.

The input IN is held low, and the impact of  $V_{SSH}$  slewing on the nodes N1, N2, and OUT is observed. The Type II level shifter shows voltage surges during 200 V/ns slewing, resulting in an erroneous output pulse. The internal nodes N1 and N2 of the Type III level shifter show pre-cursors to false

triggering, however the output remains correct. Therefore, the Type III level shifter has a significantly improved slew-rate immunity. Comparing the results of Fig. 9 and Fig. 11, it can be concluded that with the help of the additional auxiliary circuit, the Type III level shifter's power slew immunity has been improved from 60 V/ns to 200 V/ns. The cost is additional layout area for the auxiliary circuit and dynamic power dissipation during the slewing period.

#### F. STEP 4: Type IV Level Shifter With Increased Negative Power Supply Slew Immunity

The aim of Step 4 is to increase the negative slew immunity of the Type III level shifter to  $-60$  V/ns for operation during negative slewing, the scenario illustrated in Fig. 2 (b). For operation outside of the slewing periods, Fig. 2 (a), the Type I to Type III level shifters have infinite negative  $V_{SSH}$  slew rate immunity: Taking the Type III level shifter as an example, this is because parasitic capacitances  $C_1$  to  $C_4$  (Fig. 10) discharge their current into PM1, PM4, PM11, and PM14, which shifts the potential of nodes G1, G2, N5 and N6 upwards to  $V_{DDH} + V_F$ , where  $V_F$  is the forward voltage drop of parasitic diodes  $D_1$  to  $D_4$ . Therefore  $V_{GS}$  of transistors PM1, PM4, PM11 and PM14 is negative, holding them off. As a result, no parasitic currents are mirrored to nodes N1 and N2, thus the output is not affected by the negative slewing of  $V_{SSH}$ . By contrast, for operation during the slewing period, there is a maximum negative slew rate: Taking the Type III level shifter as an example, if the input IN triggers a pulse at node IN1 during negative slewing of  $V_{SSH}$  (Fig. 10), then parasitic currents  $I_{d1}$  and  $I_{d3}$  flow from the source to drain of HNM1 and HNM3 separately. At this point,  $I_{PM1} = I_{ds1} - I_{d1}$ . Above a certain slew rate,  $I_{d1}$  becomes larger than  $I_{ds1}$ , and G1 is then  $V_{DDH} + V_F$ , resulting in no current being mirrored to PM2. With  $I_{PM2}$  being zero, and similarly  $I_{NM10}$  being zero, the triggering current  $I_{NM1}$  stays zero. Therefore a pulse at node IN1 will have resulted in no change at the OUT node, representing an erroneous output.

To solve this problem, another auxiliary circuit is added to the Type III level shifter to compensate for parasitic currents  $I_{d1} - I_{d4}$  that occur during negative  $V_{SSH}$  slewing, as shown in Fig. 12. An auxiliary negative power slew immunity enhancement circuit has been added, which is composed of isolated 5V NMOS transistors TNM1-TNM6, and HV NMOS transistors HNM5 and HNM6. During negative slewing, the parasitic currents  $I_{d1} - I_{d4}$  are compensated by the mirrored currents flowing through TNM1-TNM4, since  $I_{d5} = I_{d1} = I_{d3}$ , and  $I_{d6} = I_{d2} = I_{d4}$ . TNM3 and TNM4 provide symmetry, thus ensuring that nodes N5-N8 have the same load. Both the positive and negative power slew immunity enhancement circuits operate separately during the positive and negative slewing periods, and do not interact with each other.

To show the improvement in negative  $V_{SSH}$  slewing immunity, a pulse train is applied to input IN of both Type III and Type IV level shifters, while  $V_{SSH}$  is slewing at  $-60$  V/ns, see Fig. 13. The second input pulse (uppermost plot) falls into the negative slewing period. It is apparent that the pulse



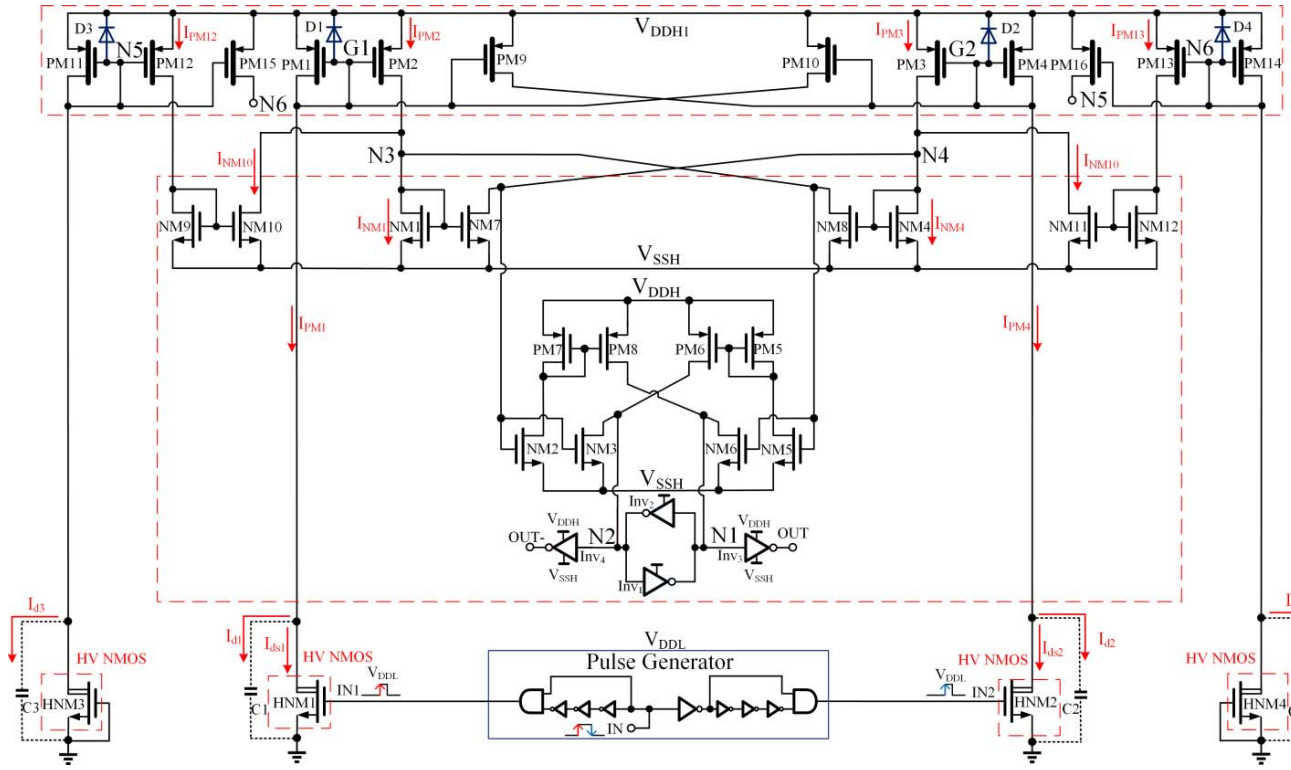


Fig. 10. Level shifter type III: level up shifter with auxiliary positive power supply slew immunity enhancement circuit (dashed boxes are Deep N-well).

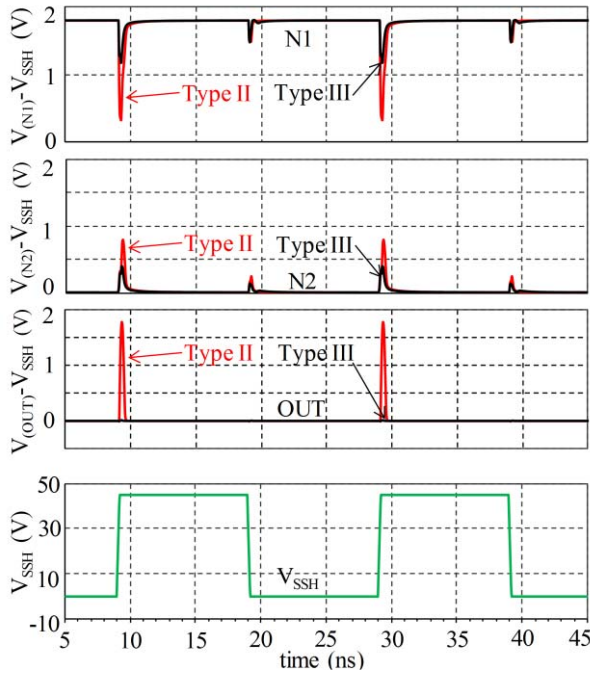


Fig. 11. Post-layout transient simulation results of Type II and Type III level shifters with a positive  $V_{SSH}$  slew rate 200V/ns.

is correctly transmitted to the output OUT of the Type IV level shifter, however it is lost in the Type III level shifter.

The PMOS transistors length of PM1-PM4 in Fig. 12 is chosen using design rules of [10]. These provide the relationship between devices length and propagation delay. The width

is chosen to be the minimum that avoids voltage overstress at the 5.5 V maximum operating voltage and 200 V/ns slew rate.

The minimum pulse width that the Type IV level shifter can transmit depends on the slowest path from the input to output. The slowest path is from IN1 to N5 (or IN2 to N6), which is limited by the low speed HV device HNM1 and the capacitance seen from its drain. The delay from IN1 to N5 is 270 ps, and the one-shot pulse width at IN1 is set to 500 ps to guarantee correct operation.

Type IV level shifter has a symmetrical circuit architecture, and therefore slew rate immunity is sensitive to mismatch. Simulation shows that with a 10% mismatch of HNM1 and HNM2, this level shifter maintains its slew immunity of 200 V/ns.

TABLE 1 shows the post-layout simulation results of the reference base-line level shifter of Fig. 3 and the four optimised level shifters developed in this section. Simulated values for  $T_R$ ,  $T_F$  and  $E_T$  are given for  $V_{DDH} = 50V$ . The positive and negative power supply slewing immunities are also given for operation outside of and during slewing. The Type I level shifter operates correctly when  $V_{SSH}$  is as low as  $-1.5V$ , but with increased  $T_R$ ,  $T_F$  and  $E_T$  compared with base-line level shifter. The trade-off between power supply slewing immunity and propagation delays can be seen. Type III level shifter has a power supply slewing immunity of 200 V/ns. Compared to base-line level shifter, this represents a 13-fold improvement in immunity, at a cost of only a 35% increase in propagation delay. The Type IV level shifter achieves 200 V/ns positive and infinite negative slew immunity for operation outside of slewing, and 200 V/ns positive and  $-60$  V/ns negative slewing immunity if operated during  $V_{SSH}$  slewing.



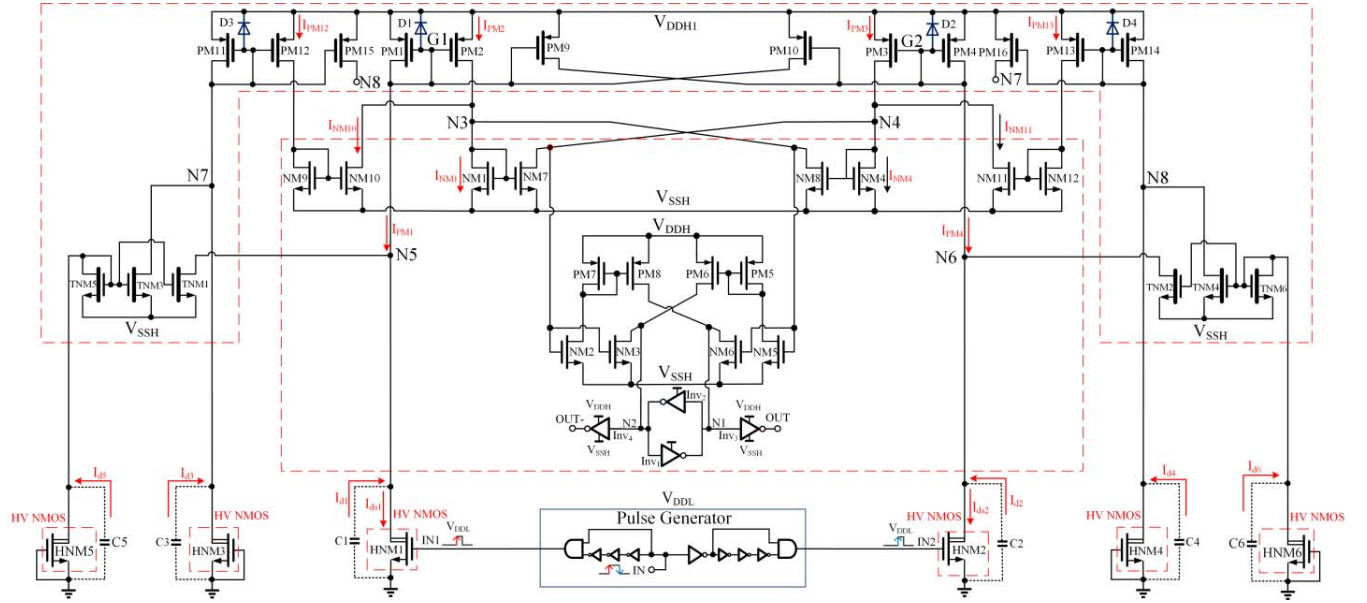


Fig. 12. Level shifter type IV: level up shifter with auxiliary positive and negative power supply slew immunity enhancement circuit (red dash boxes are Deep Nwell).

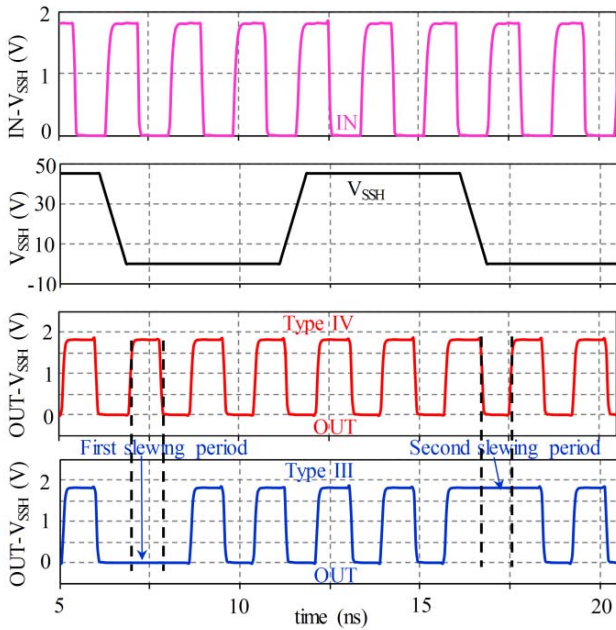


Fig. 13. Post-layout transient simulation results of Type III and Type IV with operation during  $V_{SSH}$  slewing of  $-60\text{V/ns}$ .

To implement a Type IV level shifter in SMPS shown in Fig. 1, the following design methods should be considered.

- 1) The accurate floating power rails  $V_{DDH} - V_{SSH} = 1.8\text{ V}$  and  $V_{DDH1} - V_{SSH} = 5\text{ V}$  can be generated on chip using bootstrap power supply technique of [23] with two external bootstrap capacitors for each power rail.
- 2) As Type IV level shifter is an edge-triggered level shifter, its initial output state should be set to keep the

upper GaN FET held off through power-on-reset circuit during the SMPS power up.

- 3) The high-side buffer that is driven by the level shifter is not subject to high slew rates as it is referenced to  $V_{SSH}$ , but it does add propagation delay. A careful design of this buffer is needed to balance its propagation delay and driving ability, which depends on the type of GaN FET chosen, and the speed at which it is driven.
- 4) The  $V_{SSL}$  ground bounce induced by high slewing switching current could affect the narrow one-shot pulse generated at node N1 and N2. To alleviate this problem, the ground of the level shifter should be separated from the power ground  $V_{SSL}$ .

## V. MEASUREMENT RESULTS AND COMPARISON WITH PREVIOUS WORK

This section provides measured results for the Type IV level shifter.

### A. Measurement Technique

To verify the design technique of Section IV, the final Type IV level shifter of Fig. 13 has been fabricated in an AMS 180 nm 50V HV CMOS process. The high voltage floating level shifters presented all exhibit very short propagation delays, which would make it problematic to measure the propagation delays through the die's IO pads directly, since the IO buffers are too slow. Therefore the method in [12] is used here to measure the propagation delays, where level shifters form the inverting delay cells in a ring oscillator, as shown in Fig. 14.

This ring oscillator features an oscillator loop comprising a level-up shifter in series with a level down shifter, with inversion being provided by a 2-input NAND gate. The level-down shifter is designed using the same technique as

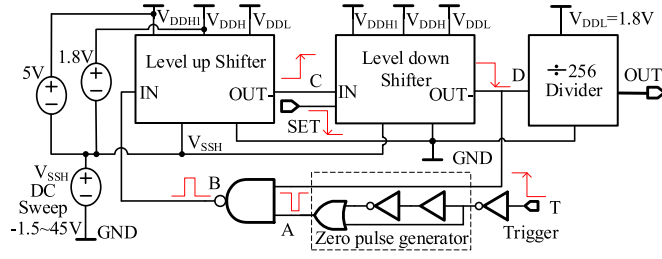


Fig. 14. Measurement set up circuit of oscillator with divider.

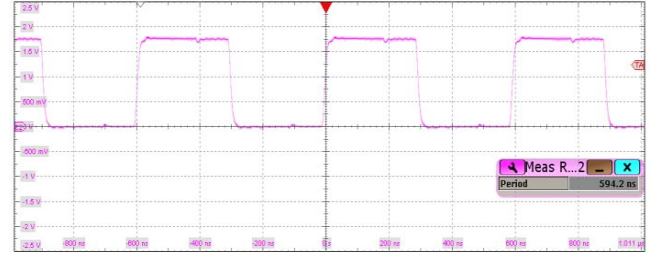


Fig. 16. Measured transient output waveform of the ring oscillator.

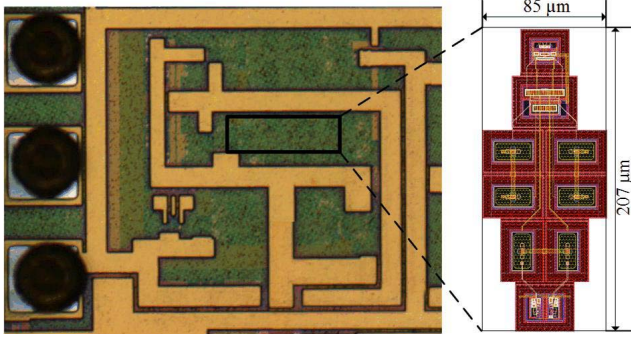


Fig. 15. Micrograph of the measurement circuit and the layout of the type IV level shifter.

the level-up shifter and has similar propagation delays. The NAND2 gate is assumed to have the same rising and falling delay time  $T_{\text{nand2}}$ . Oscillator frequency is measured via a 256 times divider driving an I/O pad. The period  $T_{\text{OSC}}$  of the oscillator is measured. The average propagation delay of level up and down shifters  $T_{\text{AVE}}$  is then

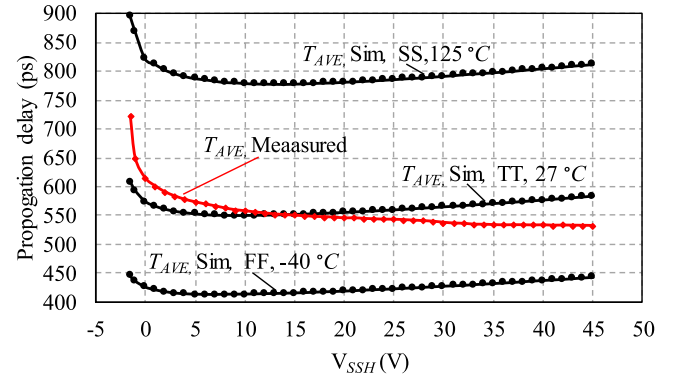
$$T_{\text{AVE}} = \frac{(T_{\text{OSC}} - 2 * 256 T_{\text{nand2}})}{4 * 256}.$$

Since the level shifters are both pulse triggered, to start oscillation, the initial stage of each level shifter state needs to be set. As shown in Fig. 14, signal SET and trigger T are transitioned to set the initial state of the oscillator and then the oscillator runs freely. SET's falling edge sets node D to  $V_{\text{DDL}}$ . Following this, node D's state is controlled by the input at node C. A rising edge at T is supplied to trigger node B and generate a one-shot pulse. This pulse signal's rising edge sets node C to  $V_{\text{SSH}}$ . When node B falls, the rising edge generates at node C, then a falling edge at node D occurs. Since the trigger signal T is already high, the NAND2 gate operates as an inverter and the oscillator starts ringing.

### B. Measurement Results

The photo micrograph of the measurement chip circuitry and the layout of tested Type IV level shifter are shown in Fig. 15. This level shifter layout area is  $207 \mu\text{m} \times 85 \mu\text{m}$ . Different active devices are built in several deep n-wells, and the spacing between deep n-wells needs to be large enough to achieve 50 V isolation. The layout needs careful size matching to obtain the improved slew-induced common mode current rejection.

Two sets of results for the Type IV level shifter are presented: On-chip measurement vs the previously presented

Fig. 17. Post-layout simulated and measured average propagation delay  $T_{\text{AVE}}$  of Type IV level shifter.

post-layout simulation results (same simulation as used for Fig. 13). All power rails are supplied from external fixed voltage sources during measurement ( $V_{\text{DDH1}} - V_{\text{SSH}} = 5\text{V}$ ,  $V_{\text{DDL}} = (V_{\text{DDH}} - V_{\text{SSH}}) = 1.8\text{V}$ ).  $V_{\text{SSH}}$  is set to the fixed values of  $-1.5\text{V}$  then a DC value from  $-1\text{V}$  to  $45\text{V}$  with a step of  $1\text{V}$  to get the measured values of  $T_{\text{AVE}}$  and Energy  $E_T$ . A typical transient waveform showing the period  $T_{\text{OSC}}$  of the oscillator in Fig. 14 is given in Fig. 16.

Fig. 17 shows simulated and measured average propagation delays  $T_{\text{AVE}}$ , against the floating power supply voltage  $V_{\text{SSH}}$ . The simulation uses the circuit of Fig. 14 to permit comparisons under the same load conditions. The measured average propagation delay  $T_{\text{AVE}}$  shows a monotonic drop from  $722\text{ps}$  to  $532\text{ps}$  as  $V_{\text{SSH}}$  increases from  $-1.5\text{V}$  to  $45\text{V}$ . The simulated  $T_{\text{AVE}}$  drops from  $608\text{ps}$  to  $549\text{ps}$  as  $V_{\text{SSH}}$  increases from  $0\text{V}$  to  $9\text{V}$ , and then increases slightly to  $583\text{ps}$  as  $V_{\text{SSH}}$  increases from  $9\text{V}$  to  $45\text{V}$ . The measured average propagation delays are within  $\pm 10\%$  of the simulated results from  $V_{\text{SSH}} = -1\text{V}$  to  $45\text{V}$  in typical condition. The discrepancy is most likely due to limited model accuracy of HV devices' voltage dependant drain to  $V_{\text{SSL}}$  or  $V_{\text{DDH}}$  parasitic capacitances.

The energy consumption per transient  $E_T$  is measured. Fig. 18 provides the simulated and measured energy consumption per transient  $E_T$  versus the floating supply voltage  $V_{\text{SSH}}$ , demonstrating a close match. The energy consumption per transient is seen to increase almost linearly with  $V_{\text{SSH}}$ . This can be explained by the trigger currents through HNM1 and HNM2 in Fig. 12 remaining almost constant, whereas  $V_{\text{DDH}}$  increases linearly.

TABLE II  
COMPARISONS WITH PREVIOUS WORK

	Process	Voltage (V)	$E_T$ (pJ)	Delay (ns)	Slew rate (V/ns)	FOM	FOM*	Layout area (mm <sup>2</sup> )	Note
[7]	0.5 $\mu$ m UHV	700	NA	20	120	0.06	NA	NA	Measured
[10]	0.18 $\mu$ m HVCMOS	20	7.2	0.37	30	0.10	23	0.005	Measured <sup>1</sup>
[12]	0.35 $\mu$ m HVCMOS	10	24 <sup>1</sup>	2.4	NA	0.69	56 <sup>1</sup>	NA	Measured <sup>1</sup>
[13]	0.35 $\mu$ m HVCMOS	20	6	3	NA	0.43	21	NA	Simulation
[18]	0.5 $\mu$ m BCD	25	50	1.7	NA	0.14	28	0.007	Simulation
[19]	0.18 $\mu$ m BiCMOS	50	NA	5	20	0.56	NA	0.036	Measured
[20]	0.5 $\mu$ m HVCMOS	40	160	2.0	40	0.1	64	0.22	Measured <sup>1</sup>
[24]	0.35 $\mu$ m HVCMOS	50	23.7	2.03	NA	0.12	23	0.049	Simulation
<b>This work</b>	<b>0.18<math>\mu</math>m HVCMOS</b>	<b>50</b>	<b>30.3</b>	<b>0.53</b>	<b>200</b>	<b>0.06</b>	<b>54</b>	<b>0.018</b>	<b>Measured</b>

FOM from [12]: (Delay)/(Process node·Voltage). Unit: (ns)/( $\mu$ m·V)

FOM\*: ( $E_T$ ·Delay)/(Process node<sup>3</sup>·Voltage). Unit: (pJ·ns)/( $\mu$ m<sup>3</sup>·V)

Note 1:  $E_T$  is simulated. Mmm<sup>2</sup>

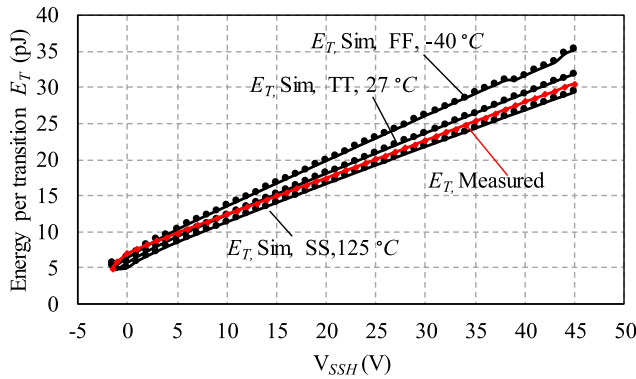


Fig. 18. Post-layout Simulated and Measured Energy per transition ( $E_T$ ) of the Type IV level shifter.

The physical measurement of slew rate immunities will require the proposed (0.018 mm<sup>2</sup>) level shifter to be embedded in a high-speed, dual-channel gate driver (around 10 mm<sup>2</sup> [9]). Here we have determined the slew rate immunity (Section III) using post-layout simulation.

### C. Figure of Merit Evaluation

TABLE 2 compares the Type IV level shifter presented in this paper with the literature. The processes, maximum operation voltage, energy consumption per transition, propagation delay, power supply slewing immunity and layout area are given. To more accurately compare the performance of level shifters based on different process and circuit topologies, a figure of merit (FOM) from [12] is used. This FOM evaluates the delay across different process nodes and operating voltages; smaller values are better. It is worth noting that the FOM includes the parameters ‘process node’ and ‘operating voltage’, both of which include area information. The floating level shifter in this paper has the lowest value of 0.06, which is a 1.7-times improvement on the next best reported level shifter. Since power dissipation is an important characteristic of level shifters, the FOM\* from [10] is also used here; higher

values are better. The level shifter in this paper has a measured FOM\* of 54, which is higher than the measured result in [10] and the simulated results in [18], [13], and [24], and similar to the measured result of [12], and smaller than the measured result in [20].

The Type IV level shifter in this paper has the highest power supply slew tolerance of 200 V/ns. The next-best slew immunity for a level shifter with sub-ns delay is only 30 V/ns

## VI. CONCLUSION

This paper presents a new 4 step method for designing ultra-high slew-rate immunity into floating voltage level shifters that meet the requirements of next-generation GaN FET drivers. By applying this method to a reported level shifter [10] the slew immunity is improved almost 7-fold, and its FOM\* is doubled. The steps produce level shifters with different trade-offs in area, slew immunity, and power supply voltage range.

The final design has been fabricated in 180 nm ASIC technology. Its measured average propagation delay is below 722 ps over the entire range of operating voltage (−1.5 V to 45V), and it operates correctly under power supply slew rates of 200 V/ns. Its figure-of-merit is 1.7 times better than the next best reported prior art. The level shifter can be used in commercial GaN drivers which apply step functions to the GaN gate where it achieves slew immunities of +200 V/ns and  $-\infty$ , and in multi MHz converters due to its sub-ns propagation delay. It is also suitable for use in emerging active gate drivers that apply a profiled signal to the GaN gate, as it achieves slew immunities of +200 V/ns and −60 V/ns even when operated during slewing.

## REFERENCES

- [1] S. Bandyopadhyay, B. Neidorff, D. Freeman, and A. P. Chandrakasan, “90.6% efficient 11 MHz 22 W LED driver using GaN FETs and burst-mode controller with 0.96 power factor,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 368–369.
- [2] M. K. Song, L. Chen, J. Sankman, S. Terry, and D. Ma, “A 20 V 8.4 W 20 MHz four-phase GaN DC-DC converter with fully on-chip dual-SR bootstrapped GaN FET driver achieving 4 ns constant propagation delay and 1 ns switching rise time,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.



- [3] X. Ke, J. Sankman, M. K. Song, P. Forghani, and D. B. Ma, "A 3-to-40 V 10-to-30 MHz automotive-use GaN driver with active BST balancing and VSW dual-edge dead-time modulation achieving 8.3% efficiency improvement and 3.4 ns constant propagation delay," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan./Feb. 2016, pp. 302–304.
- [4] Y. Wang, W. Kim, Z. Zhang, J. Calata, and K. D. Ngo, "Experience with 1 to 3 megahertz power conversion using eGaN FETs," in *Proc. IEEE 28th Annu. Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2013, pp. 532–539.
- [5] J. Strydom and D. Reusch, "Design and evaluation of a 10 MHz gallium nitride based 42 V DC-DC converter," in *Proc. 29th IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2014, pp. 1510–1516.
- [6] D. Reusch, D. Gilham, Y. Su, and F. C. Lee, "Gallium nitride based 3D integrated non-isolated point of load module," in *Proc. IEEE 27th Annu. Appl. Power Electron. Conf. Expo. (APEC)*, Feb. 2012, pp. 38–45.
- [7] H.-A. Yang *et al.*, "120 V/ns output slew rate enhancement technique and high voltage clamping circuit in high integrated gate driver for power GaN FETs" in *Proc. 41st Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2015, pp. 291–294.
- [8] K. Miyazaki *et al.*, "General-purpose clocked gate driver IC with programmable 63-level drivability to optimize overshoot and energy loss in switching by a simulated annealing algorithm," *IEEE Trans. Ind. Appl.*, vol. 53, no. 3, pp. 2350–2357, May/Jun. 2017.
- [9] J. Wang, D. Liu, H. C. P. Dymond, J. J. O. Dalton, and B. H. Stark, "Crosstalk suppression in a 650-V GaN FET bridgeleg converter using 6.7-GHz active gate driver," in *Proc. IEEE Energy Conversion Congr. Expo. (ECCE)*, Oct. 2017, pp. 1955–1960.
- [10] D. Liu, S. J. Hollis, H. C. P. Dymond, N. McNeill, and B. H. Stark, "Design of 370-ps delay floating-voltage level shifters with 30-V/ns power supply slew tolerance," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 7, pp. 688–692, Jul. 2016.
- [11] B.-D. Choi, "Enhancement of current driving capability in data driver ICs for plasma display panels," *IEEE Trans. Consum. Electron.*, vol. 55, no. 3, pp. 992–997, Aug. 2009.
- [12] Y. Moghe, T. Lehmann, and T. Piessens, "Nanosecond delay floating high voltage level shifters in a 0.35  $\mu\text{m}$  HV-CMOS technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 485–497, Feb. 2011.
- [13] T. Lehmann, "Design of fast low-power floating high-voltage level-shifters," *Electron. Lett.*, vol. 50, no. 3, pp. 202–204, Jan. 2014.
- [14] J.-F. Richard, B. Lessard, R. Meingan, S. Martel, and Y. Savaria, "high voltage interfaces for CMOS/DMOS technologies," in *Proc. IEEE Northeast Workshop Circuits Syst.*, Montreal, QC, Canada, 2003, pp. 93–96.
- [15] M. Khorasani *et al.*, "Low-power static and dynamic high-voltage CMOS level-shifter circuits," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2008, pp. 1946–1949.
- [16] P. S. Swain, M. Shrivastava, H. Gossner, and M. S. Baghini, "Device-circuit co-design for beyond 1 GHz 5 V level shifter using DeMOS transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3827–3834, Nov. 2013.
- [17] P. S. Swain, M. S. Baghini, V. R. Rao, M. Shrivastava, and H. Gossner, "Device-circuit co-design for high performance level shifter by limiting quasi-saturation effects in advanced DeMOS transistors," in *Proc. IEEE Int. Nanoelectron. Conf. (INEC)*, May 2016, pp. 1–2.
- [18] Y.-M. Li, C.-B. Wen, B. Yuan, L.-M. Wen, and Q. Ye, "A high speed and power-efficient level shifter for high voltage buck converter drivers," in *Proc. 10th IEEE Int. Conf. Solid-State Integr. Circuit Technol.*, Nov. 2010, pp. 309–311.
- [19] J. Wittmann, T. Rosahl, and B. Wicht, "A 50 V high-speed level shifter with high DV/DT immunity for multi-MHz DCDC converters," in *Proc. 40th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2014, pp. 151–154.
- [20] Z. Liu, L. Cong, and H. Lee, "Design of on-chip gate drivers with power-efficient high-speed level shifting and dynamic timing control for high-voltage synchronous switching power converters," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1463–1477, Jun. 2015.
- [21] M. Akahane *et al.*, "A new level up shifter for HVICs with high noise tolerance," in *Proc. Int. Power Electron. Conf. (IPEC-Hiroshima-ECCE ASIA)*, May 2014, pp. 2302–2309.
- [22] Efficient Power Conversion. (2013). *EPC2015—Enhancement Mode Power Transistor*. [Online]. Available: <https://epc-co.com>
- [23] H. Ma, R. van der Zee, and B. Nauta, "Design and analysis of a high-efficiency high-voltage class-D power output stage," *IEEE J. Solid-State Circuits*, vol. 49, no. 7, pp. 1514–1524, Jul. 2014.
- [24] D. Ø. Larsen, P. L. Muntal, I. H. Jørgensen, and E. Bruun, "High-voltage pulse-triggered SR latch level-shifter design considerations," in *Proc. NORCHIP*, Oct. 2014, pp. 1–6.



**Dawei Liu** received the B.S. and M.S. degrees in microelectronics from the Harbin Institute of Technology, Harbin, China, in 2005, and 2007, respectively, and the Ph.D. degree in electrical and electronic engineering from the University of Bristol, Bristol, U.K., in 2017. He is currently with the Electrical Energy Management Group, University of Bristol, as a Senior Research Associate. His research interests are analogue and power IC design, and high-speed gate driver design.



**Simon J. Hollis** received the M.A. and Ph.D. degrees in computer science from Cambridge University, U.K., in 2004 and 2007, respectively. From 2007 to 2015, he was a Lecturer in computer science with the University of Bristol, U.K., researching energy efficient computing, many-core systems, processor energy measurement, and high-speed programmable drivers. From 2016 to 2018, he developed milliwatt-class neuromorphic machine-learning systems at IBM Research, Almaden Labs, San Jose, CA, USA. He is currently with Xilinx Inc., San Jose, developing high-performance FPGA machine-learning architectures, compilers and tool-chains for the Versal architecture.



**Bernard H. Stark** received the M.S. degree in electrical engineering from the Swiss Federal Institute of Technology, Zürich, in 1995, and the Ph.D. degree in engineering from Cambridge University, U.K., in 2000.

He spent time as a Junior Research Fellow with the St. Hugh's College, Oxford, U.K., and as a member of the Control and Power Group, Imperial College, London, U.K. He is currently a Professor of electrical and electronic engineering with the University of Bristol, and a member of the Electrical

Energy Management Research Group. His research interests include renewable power sources and power electronics.